88. The ballasting circuit of Claim 86 in which the inverter includes

a periodically switched transistor, and

means including a saturable inductor for controlling the switching period of said transistors.

89. The improvement of Claim 86 including means for adjusting the inductance value of said inductor to adjust the amount of light output of said gas discharge lamp.

90. In a half-bridge inverter circuit adapted to be powered from a DC voltage to provide a substantially squarewave output voltage across a pair of output terminals, said DC voltage being derived from the AC voltage present across a pair of regular electric utility power lines, said inverter circuit comprising two series-connected capacitors connected in parallel with two series-connected transistors, one of said output terminals being the point of connection between the two series-connected capacitors, the improvement comprising:

two single-wave rectifiers connected in opposite polarities from one line of said pair of power lines to opposite ends of the two series-connected capacitors; and

a conductor connected between the other line of said pair of power lines to the point of connection between the two series-connected capacitors, said conductor directly connecting one of the inverter output terminals with one of the power lines to reference it thereto.

91. The ballasting circuit of Claim 90 including means for connecting a gas discharge lamp in circuit with said output terminals, said connecting means comprising means for limiting the current provided to said gas discharge lamp.

92. The ballasting circuit of Claim 91 wherein said current limiting means comprises a series-combination of an inductor and a capacitor.

93. In an inverter having a pair of transistors, the improvement comprising:

a pair of output terminals;

means including a saturable inductor connected with said transistors for causing alternate conduction thereof to produce a substantially squarewave voltage across the pair of output terminals;

an LC series circuit connected across said pair of output terminals; and

means for connecting a load in parallel circuit with one of the elements of said series circuit.

94. The inverter of Claim 93 in which said LC series circuit has a natural resonance frequency that is substantially equal to or lower than the fundamental frequency of said squarewave voltage.

95. The inverter of Claim 94 wherein said load is a gas discharge lamp.

96. The inverter of Claim 95 wherein said gas discharge lamp is connected in parallel with the capacitive element of said LC series circuit.

97. The inverter of Claim 96 including means for adjusting the inductive element of said LC series circuit to adjust the light output of said gas discharge lamp.

98. In an inverter adapted to provide a voltage across a pair of output terminals, the improvement comprising:

a load releasibly connected with said pair of output terminals; and

means for disabling the inverter from providing said voltage across said pair of output terminals whenever the load is disconnected therefrom, thereby rendering the output terminals free from electric shock hazard whenever the load is disconnected.

99. The inverter of Claim 98 in which said inverter includes an inductor in circuit with said output terminals.

100. The inverter of Claim 99 wherein said load includes a capacitive reactance.

101. The inverter of Claim 100 wherein said load also includes a gas discharge lamp.

102. The inverter of Claim 98 including a feedback path for enabling said inverter to self-oscillate.

103. The inverter of Claim 102 in which said feedback path is interrupted whenever the load is disconnected.

104. In a fluorescent lamp ballast having two output terminals for connection with two input terminals of a fluorescent lamp, said ballast providing suitable starting and operating voltages for said fluorescent lamp and said input terminals having a capacitor connected in circuit therewith, the improvement comprising:

means for releasibly connecting said fluorescent lamp in circuit with said two output terminals; and

means for preventing said starting and operating voltages from appearing across said output terminals except when the fluorescent lamp is connected therewith, thereby rendering the output terminals substantially free from electric shock hazard whenever the fluorescent lamp is disconnected.

105. In a half-bridge inverter circuit adapted to be powered from a source of DC voltage, said circuit having a pair of series-connected transistors connected across two output terminals of a source of DC voltage said transistors being interconnected at a point and said circuit providing an inverter output between said point and one of said output terminals, the improvement comprising:

a load releasibly connected with said inverter output;

means for providing a voltage across said inverter output whenever the load is connected therewith, and

means for preventing a voltage from appearing across said inverter output whenever the load is not connected, thereby rendering the inverter output free from electric shock hazard when-

ever the load is disconnected.

106. A half bridge inverter circuit for providing a substantially squarewave output voltage from a source of DC voltage, said source having output terminals across which said DC voltage is produced, comprising:

two transistors connected in series across two of said output terminals;

means for interconnecting the two transistors at a point;

a series-combination of an inductor and a capacitor connected between said point and one of the output terminals of said DC voltage source, the natural resonant frequency of said series-combination being lower than the lowest frequency component of said squarewave output voltage; and

a load connected in parallel circuit with said capacitor to receive a voltage thereacross which is transformed in amplitude and waveshape compared with the voltage present between said point ~~and one of the terminals of said source of DC voltage~~.

107. The half bridge inverter circuit of Claim 106 including means for varying the inductance of said inductor to vary the magnitude of the voltage provided across the load.

108. The half bridge inverter circuit of Claim 107 wherein the load comprises a gas discharge lamp.

109. In an inverter circuit for providing power to a load and having a positive feedback path for providing self-oscillating inverter action, the improvement comprising:

means for releasibly connecting said load to the inverter circuit; and

means for interrupting the positive feedback path, and thereby stopping the inverter action, whenever the load is disconnected from the inverter circuit.

110. In a ballasting circuit for a gas discharge lamp having an inverter for receipt of power from a source of DC voltage to

provide a substantially squarewave voltage output across a pair of terminals, the improvement comprising:

means including an inductor for connecting said gas discharge lamp in circuit with said pair of output terminals, said inductor limiting the current supplied to the lamp; and

means including a capacitor connected in parallel with said lamp for improving the power factor by which power is drawn from said pair of output terminals.

111. A circuit operable from a source of alternating voltage for ballasting a gas discharge lamp, comprising:

a series combination of an inductor and a capacitor, said series combination connected across said source of alternating voltage and having a natural resonant frequency which is substantially equal to or lower than the lowest frequency component of said alternating voltage;

means for connecting the gas discharge lamp in parallel circuit with said capacitor; and

means for adjusting the inductance of said inductor to adjust the amount of power applied to said lamp.

112. In an inverter circuit having two transistors connected in parallel, push-pull configuration and each having a collector for providing a substantially squarewave voltage between said collectors, the improvement comprising:

a series-combination of an inductor and a capacitor connected directly between the two collectors, the natural series resonant frequency of said series-combination being substantially equal to or lower than the lowest frequency component present in said squarewave voltage; and

a load connected in parallel circuit with said capacitor which causes the voltage thereacross to be transformed in amplitude and waveshap relative to the voltage present between the two collectors to provide improved power factor loading for the inverter and to have a reduced amount of higher frequency components rela-